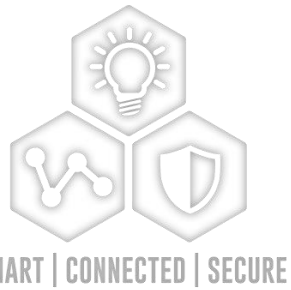
World’s Smallest FPGA SoC

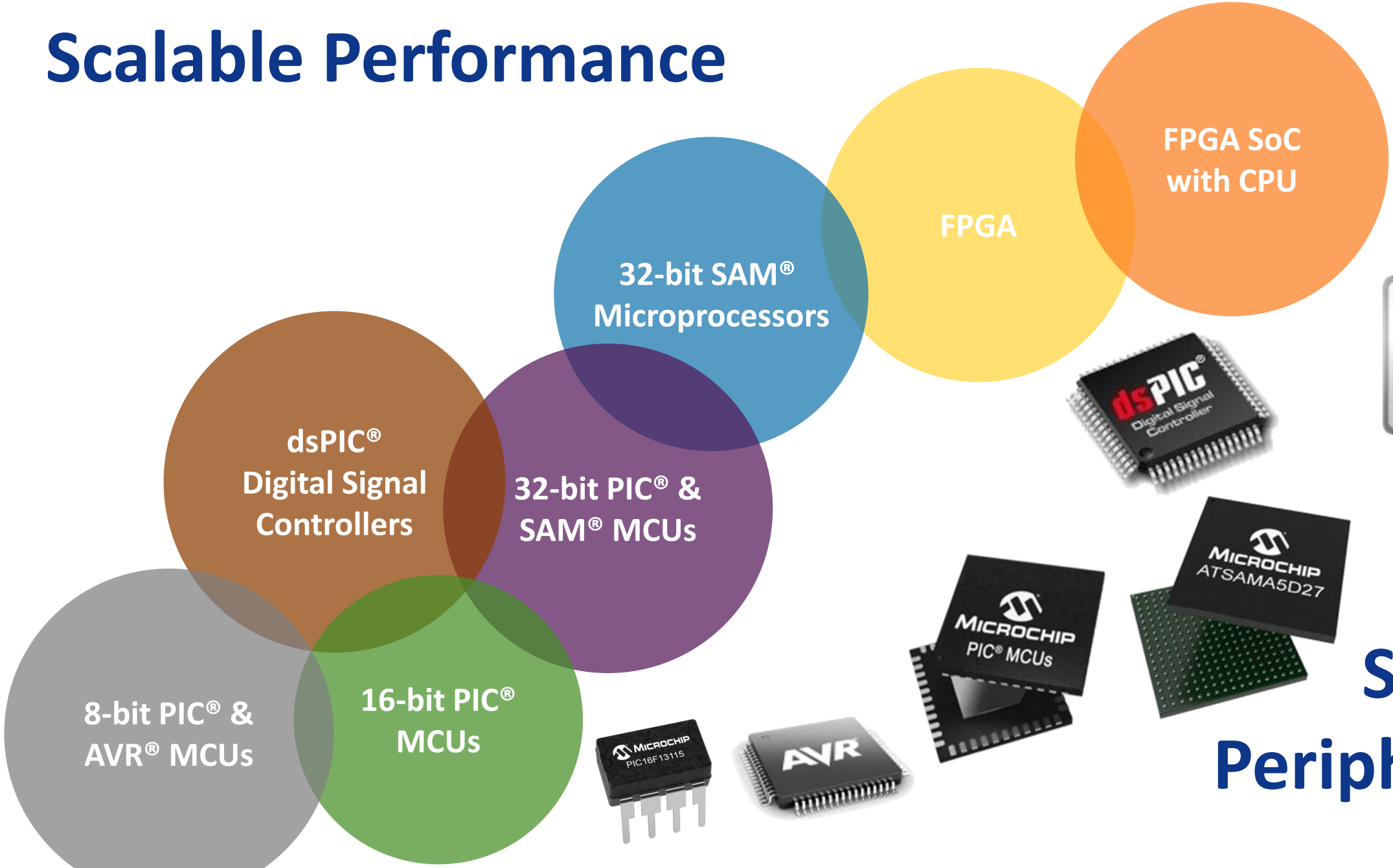
A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



Attila Kolinger

Apr 2024

Scalable Performance



Smart Peripherals

MICROCHIP

Why Use FPGA SoCs?

Safer CI/CD

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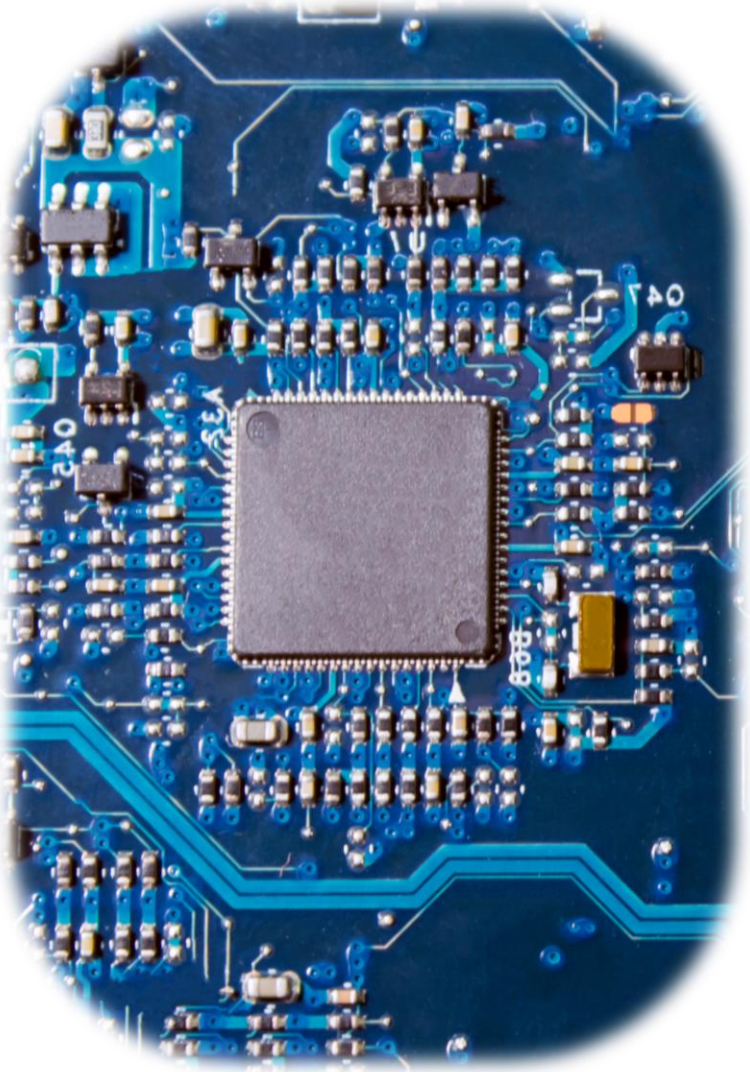
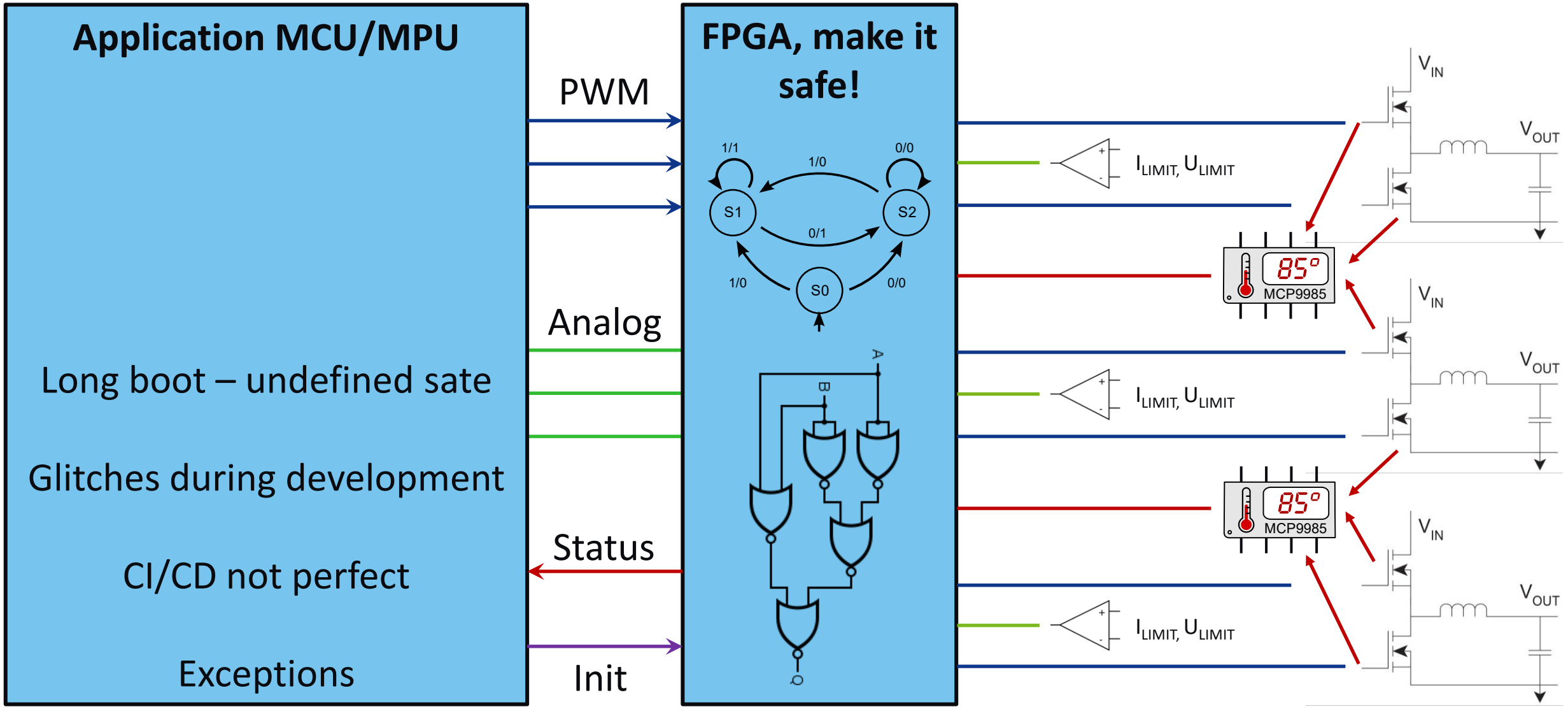
Should You Use an FPGA SoC?

YES! If you …

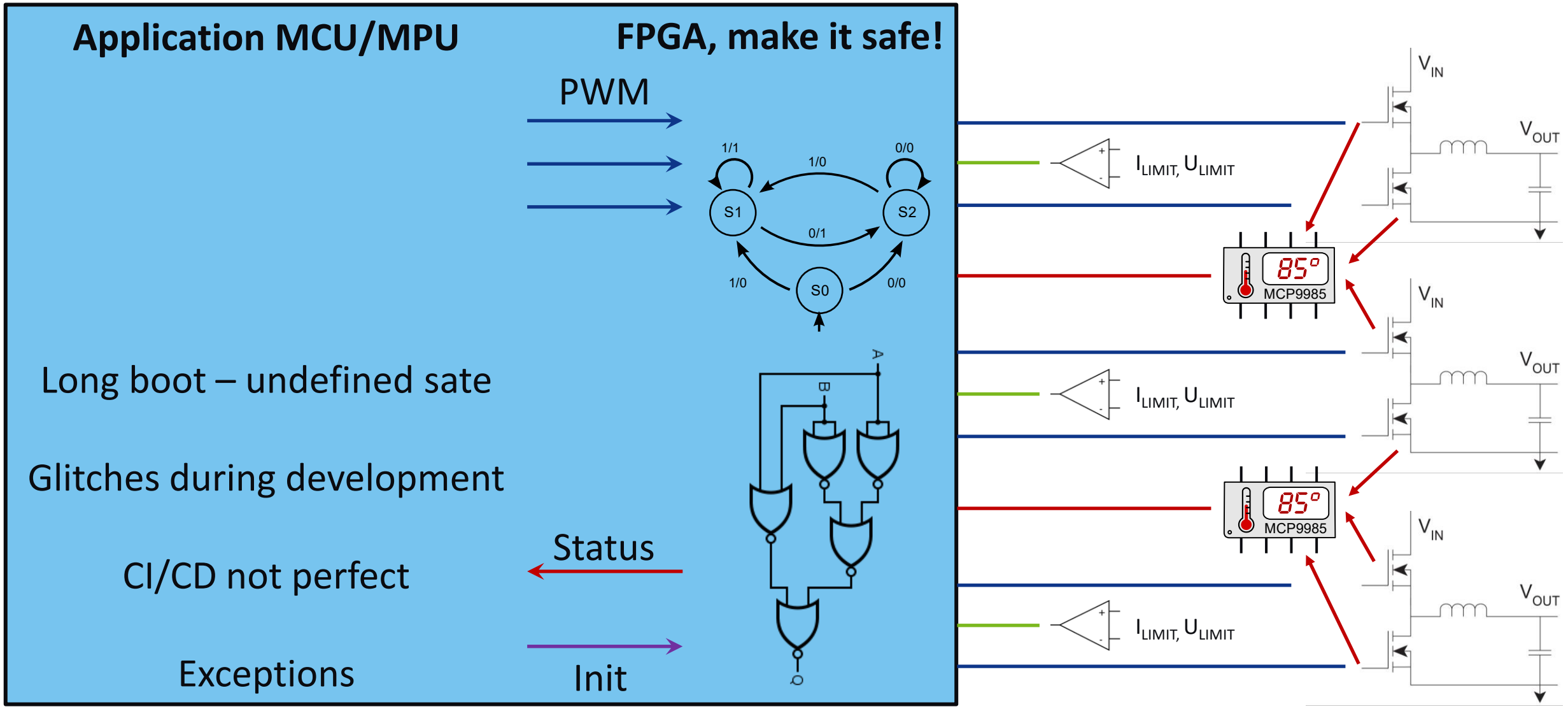
- need parallel processing
- might need PCB rewiring
- need a lot of glue logic
- have hardware that is safety critical
- demand software independent HW
- are doing pre-development
- create new MCU peripherals
- must change existing peripheral behaviour
- run “C” code in an FPGA



Unleash FW Developers



FPGA SoC Solution



FPGA SoC with CPU

The Two Extremes

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FPGA SoC Redefined

- **PolarFire SoC FPGAs**
  - Deterministic, coherent 64-bit multi-core RISC-V CPU
  - 25K to 460K LEs in FLASH
  - 12.7 Gbps transceivers
  - Up to 50% lower power than alternatives
  - Integrated DDR3/4, LPDDR3/4 controller and PHY

- **PIC16F131×× SoC**
  - Deterministic 8-bit CPU
  - 32 logic elements (RAM) Verilog and Schematics
  - Frozen FPGA blocks (UART, Timer, I²C, etc.)
  - On-board analog peripherals & True 5V (1.8V … 5.5V)
  - From 8pin package (including DIP)

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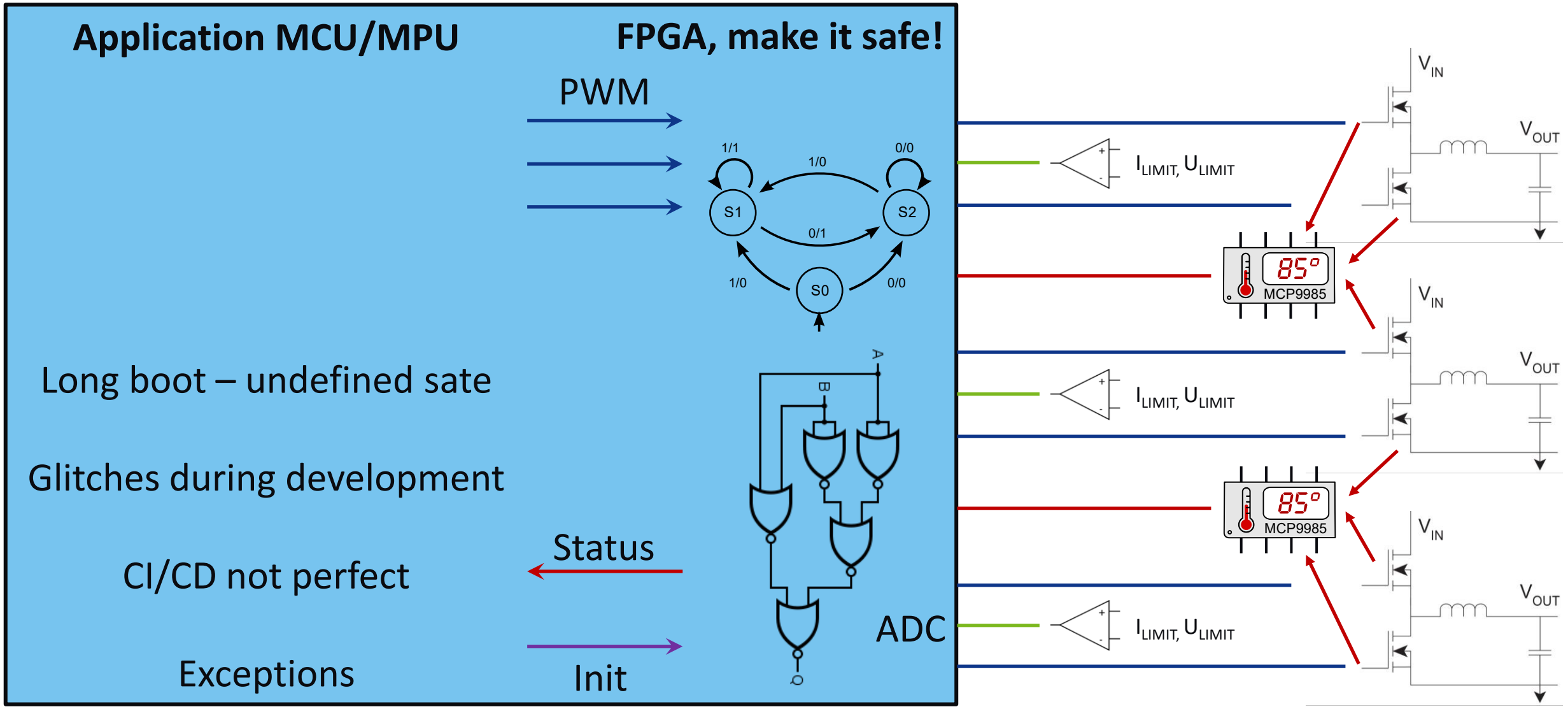
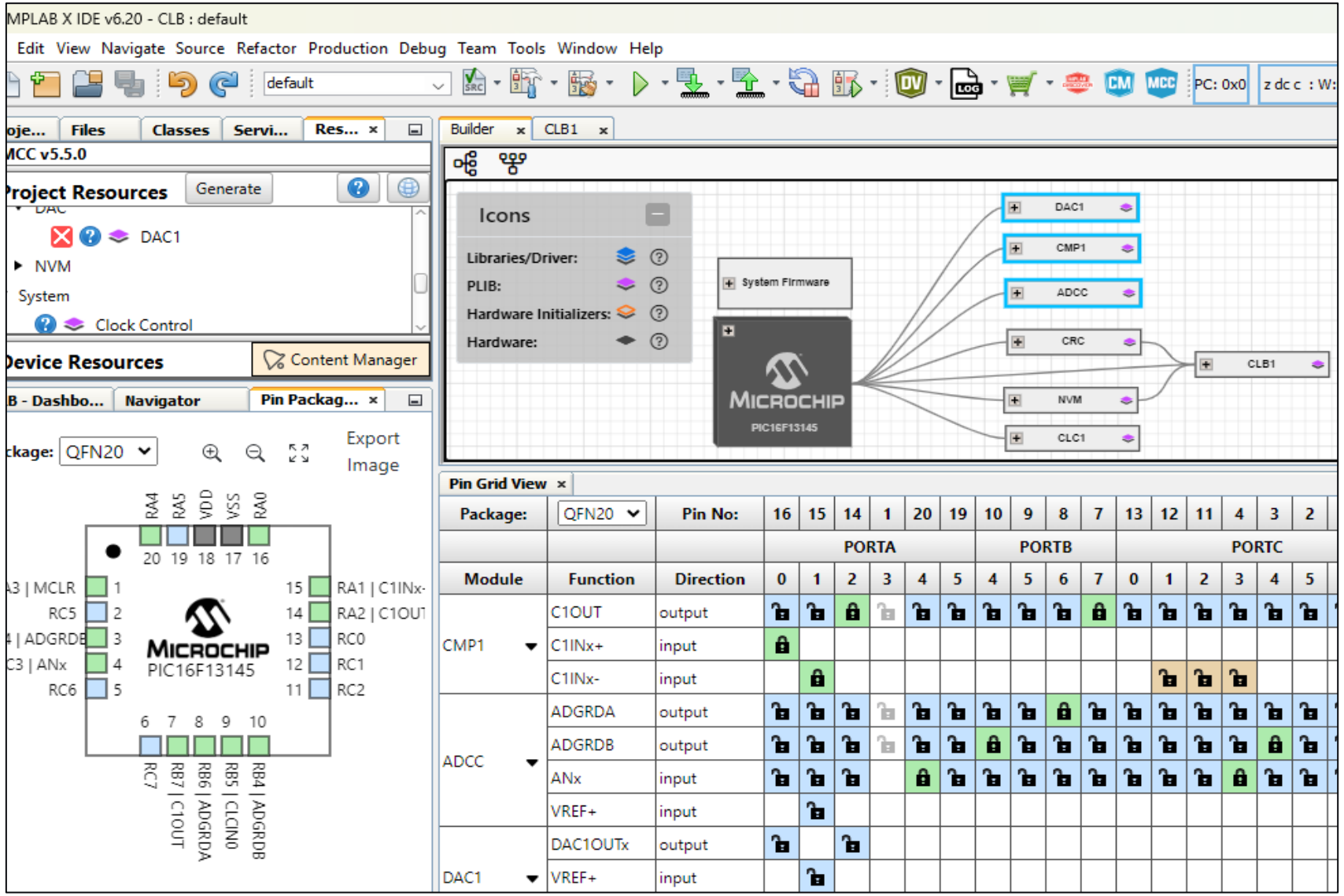
8bit FPGA SoC Solution



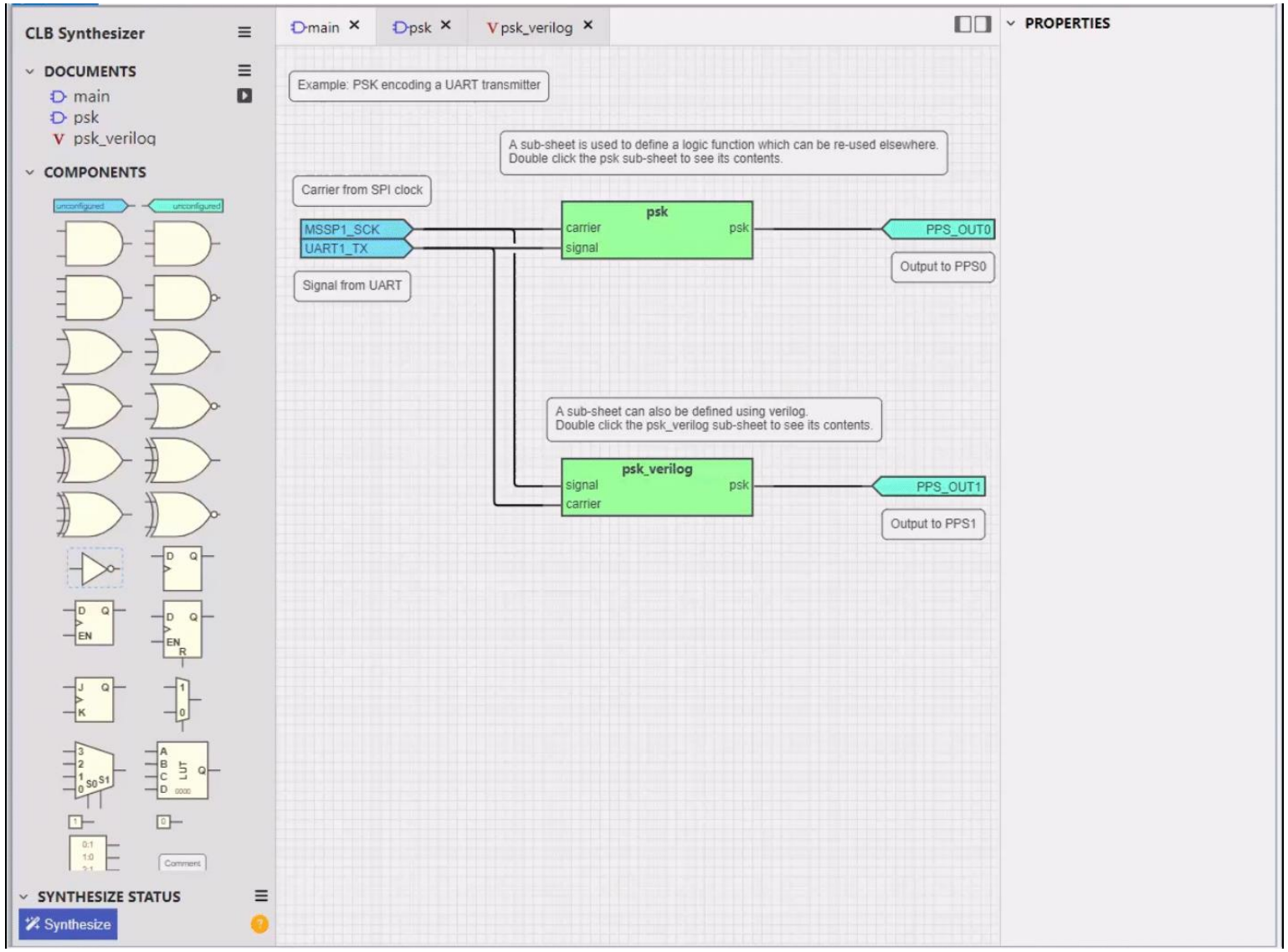
Configuration Process - MCC Melody

- **Clock config**
- **Add frozen blocks**
  - UART, I²C, TMR …
- **Add analog**
  - ADCC, DAC, …
- **Add CLB (FPGA)**

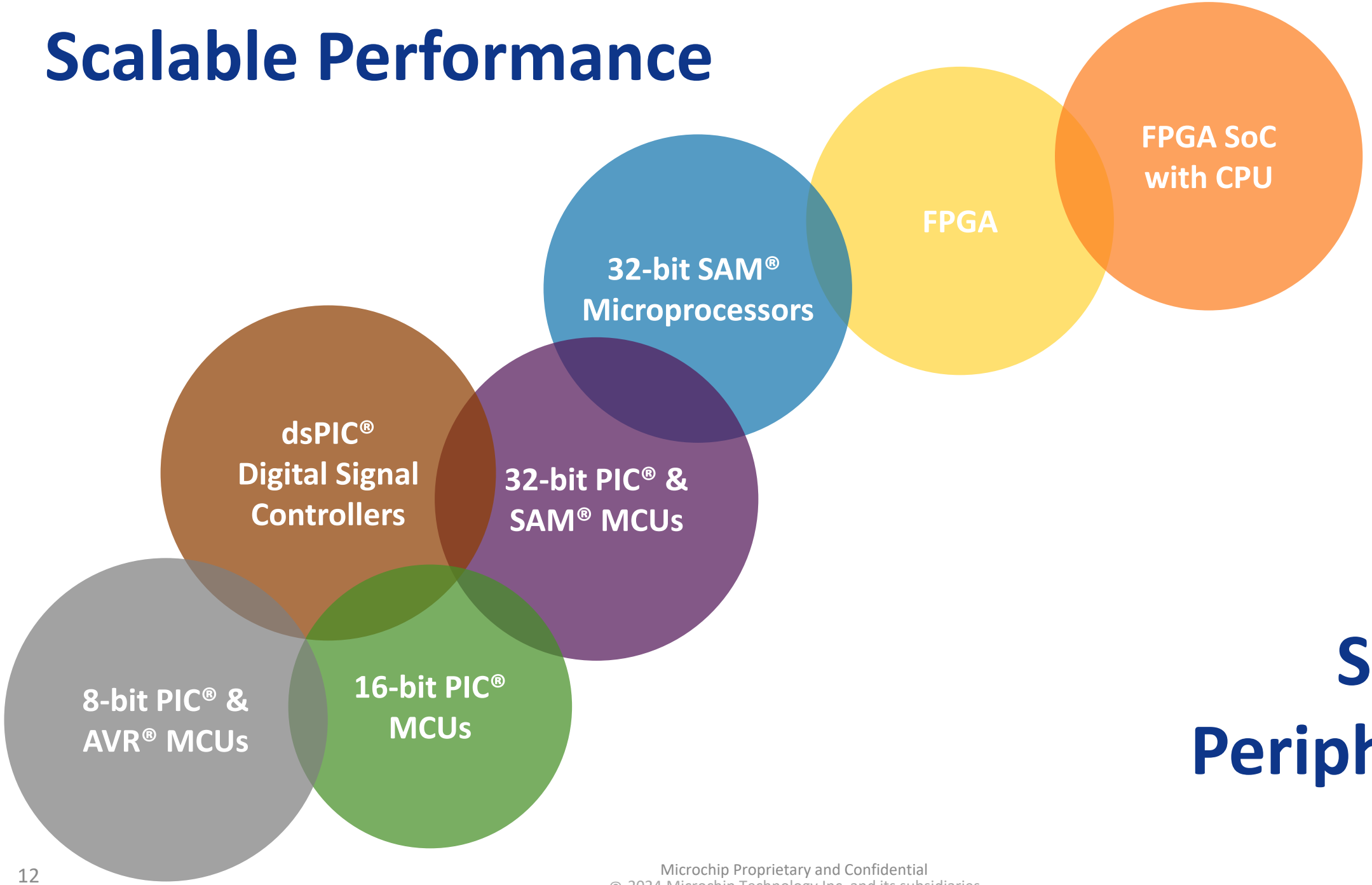


Configuration Process - MCC Melody

- Clock config
- Add frozen blocks
  - UART, I²C, TMR …
- Add analog
  - ADCC, DAC, …
- Add CLB (FPGA)
- **Create FPGA design**
- **Synthesize**
- **Configure GPIO**
- **Generate Melody code**



Scalable Performance



Smart Peripherals

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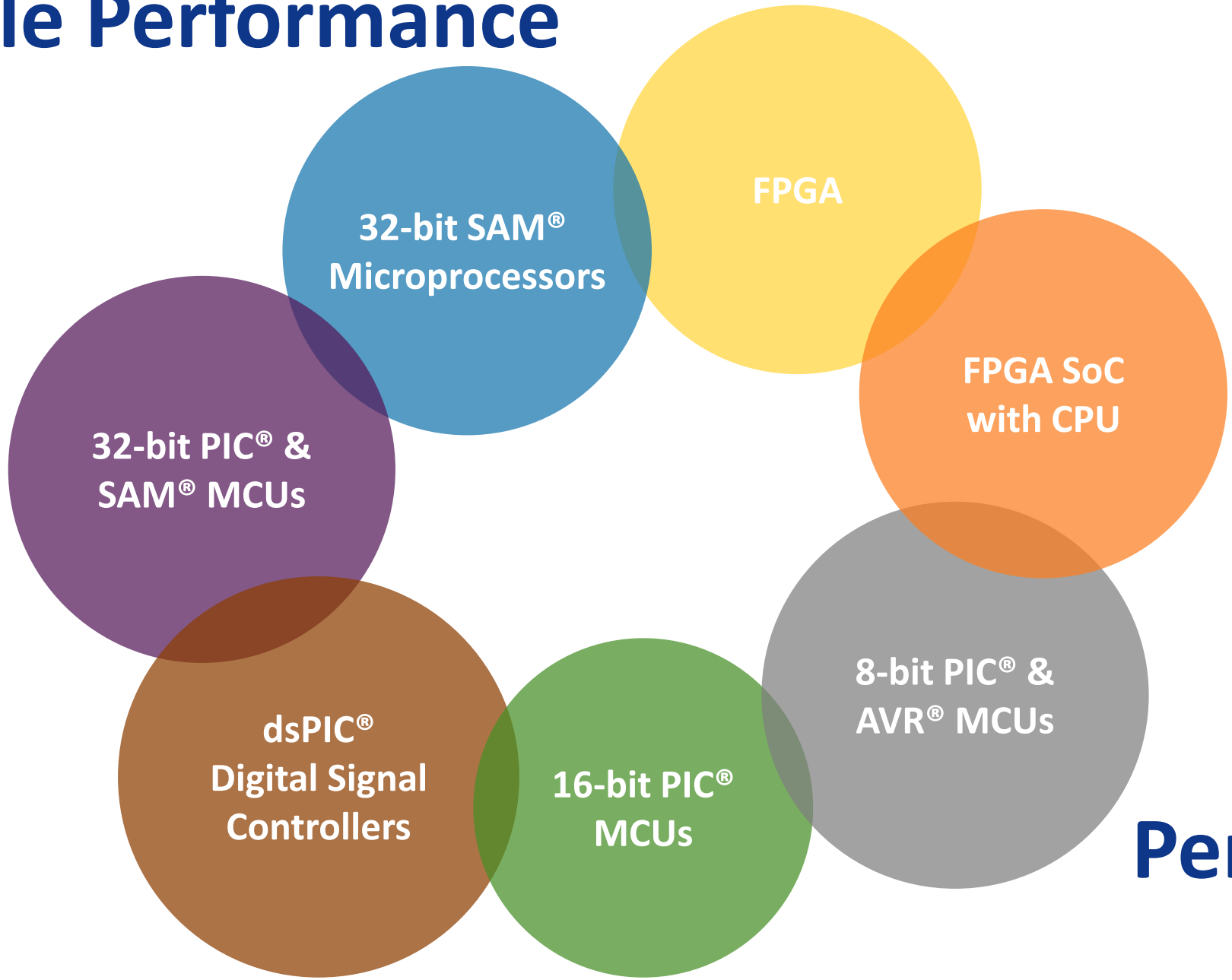
Scalable Performance



Smart Peripherals

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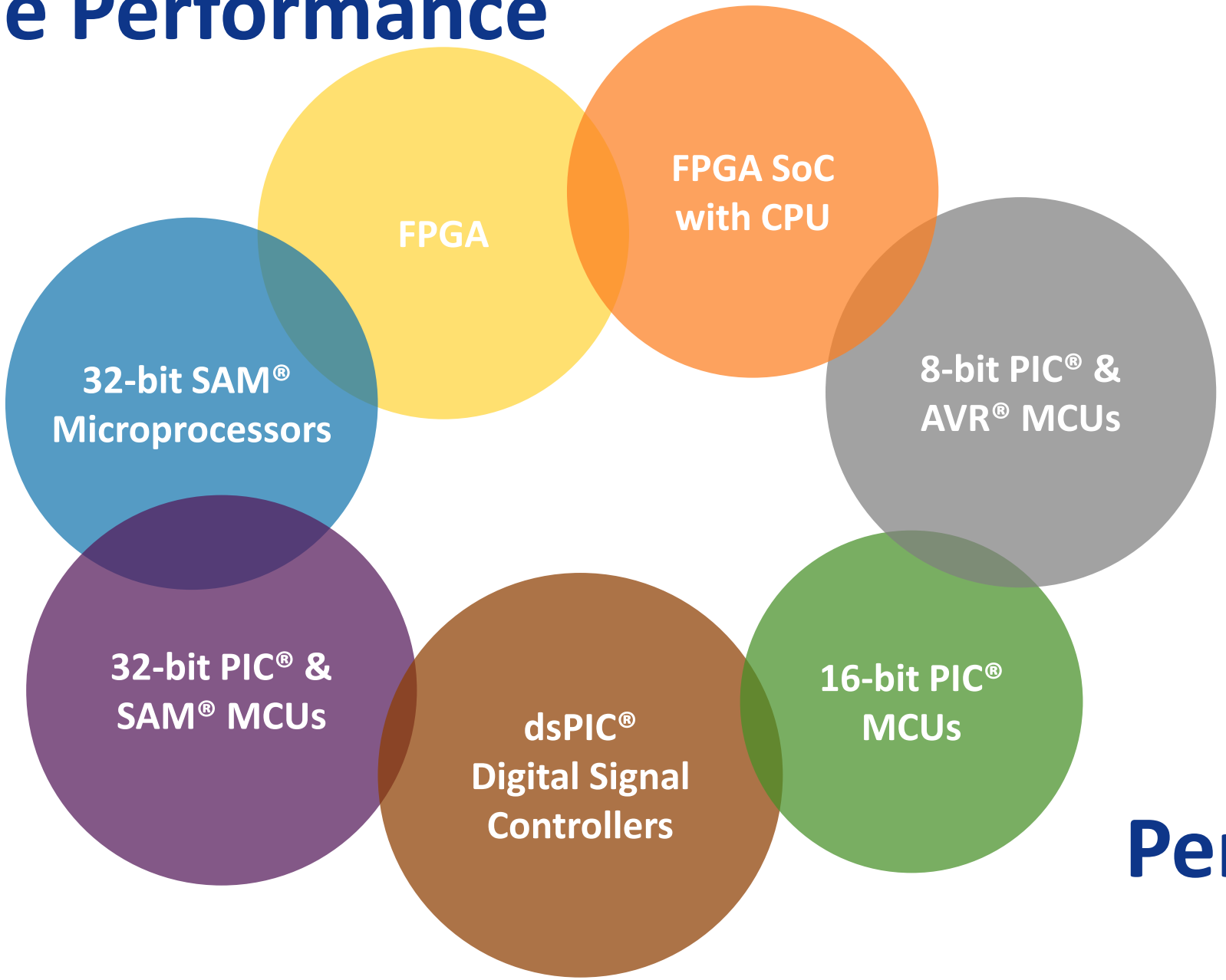
Scalable Performance



Smart Peripherals

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Thank You!

Any Questions?